

ABSTRACT

Systems and techniques for improved bus control, which may be particularly useful for double data rate (DDR) data transfer. A circuit may include a clock transmitter in communication with a clock bus, a clock receiver in communication with the clock bus, and a driver in communication with the clock bus. The driver may drive a voltage of the clock bus to a first voltage level when the clock transmitter is not transmitting a clock signal on the clock bus and the clock receiver is not receiving a clock signal on the clock bus.

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